Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **+**
2. **–**
3. **N/C**
4. **N/C**
5. **N/C**
6. **N/C**
7. **N/C**

**.030”**

**5**

**6**

**7**

**1**

**4**

**3**

**2**

**L**

**M**

**4**

**0**

**4**

**0**

**C**

**DIE ID**

**.030”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .003” X .003” min.**

**Backside Potential:**

**Mask Ref: LM4040C**

**APPROVED BY: DK DIE SIZE .030” X .030” DATE: 7/7/22**

**MFG: NATIONAL THICKNESS .020” P/N: LM4040A1-4.1**

**DG 10.1.2**

#### Rev B, 7/1